CS315-01 Advanced Architecture / Final Review

Project07

Advanced Arch

Final Review

Digital Design

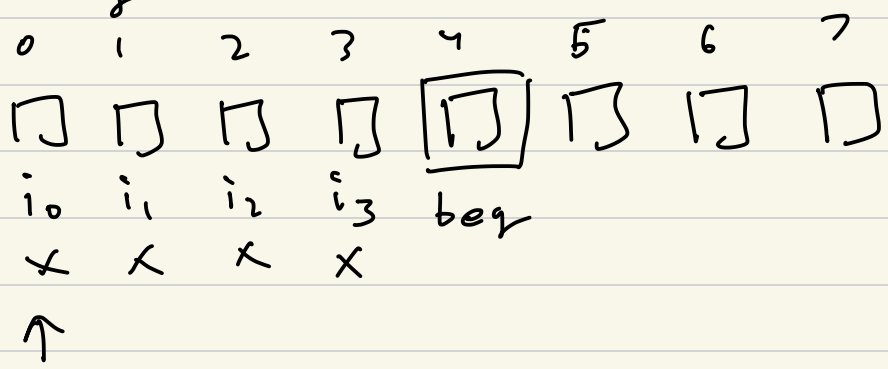
Schematic Design

HDL Hardware Description Languages

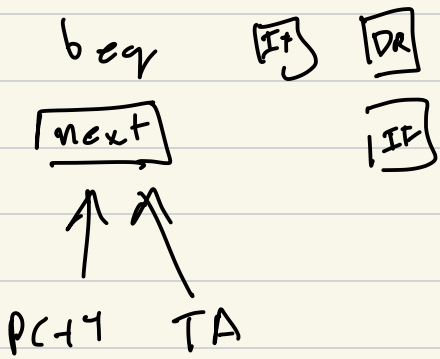
Verilog VHDL (IEEE)

CHISEL (Scala)

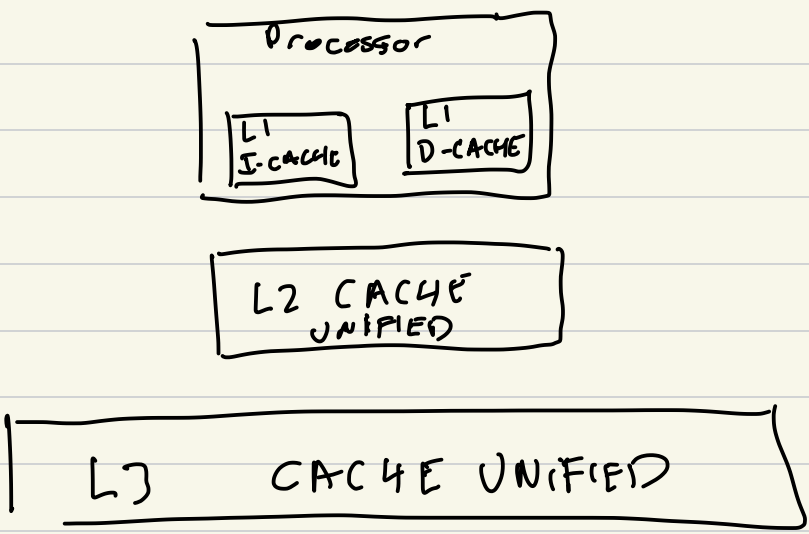
Pipelining



Branch Prediction



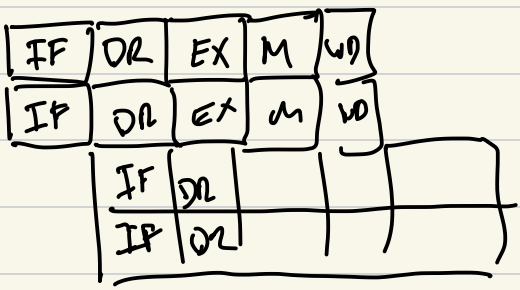
Caches



Super scalar execution

Two pipelines

```
add t0, t1, t2
sub a0, a1, a2
```

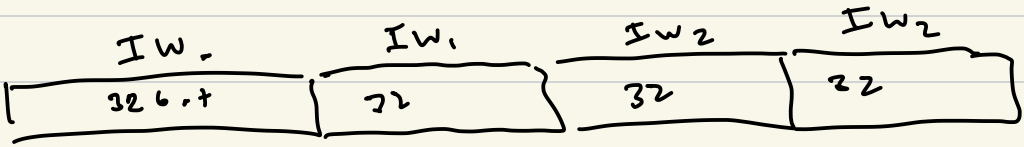


Multiple issue

VLIW - Very large Instruction Word

EPIC - Explicitly parallel Instruction Set Comp (Intel)

Itanium



Out of Order Execution

```
ld   t0, (t1)
add  t2, t3, t4
mul  s0, s1, s2
```

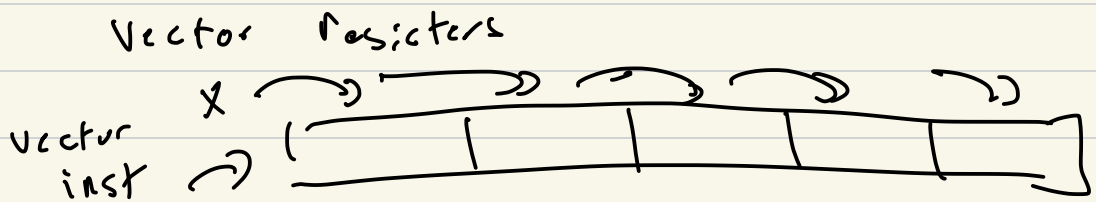
Commit stage

Speculative Execution:

Multicore

Vector Instructions SIMD

single instruction multiple data



GPU