Advanced Architecture / Final Review C5315-01 Project07 Advanced Arch Final Review Digital Design Schemetic Design HDL Hardware Description languages Verilog VHDL (IEEE) CHISEL (Scala) Pipelining 3 4 5 6 7 DDDDDDD io il iz is beg

Branch Prediction

| beg FT TR |
|---------------------|
| Mext III |
| |
| PC+4 TA |
| (aches |
| D-CACHE D-CACHE |
| L2 CACHE UNIPLED |
| UNIPIED |
| L) CACHE UNIFIED |

Super scalar execution

Tw. pipelines

add to, E1, E2 IF OR EX M 40 Sub a0, a1, a2 IF OR EX M 10

Multiple issue

ULIW - Very lunge Instruction Ward EPIC - Explicitly promuled Instruction SetComp (Intel)

Itanium

IW. 1W. 32 22

Out of Order Execution

| d to, (4)

[ald t2, t3, t4]

[mol 80,81,82]

(ommit stage

Multicore

Speculative Execution:

Vector Instructions SIMD

sinstruction multiple data

Vector Posicters

